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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/990,840	11/21/2001	Peter Irma August Barri	RAL920000112US2	3016

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EXAMINER	
PEUGH, BRIAN R	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/990,840	BARRI ET AL.	
	Examiner	Art Unit	
	Brian R. Peugh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,24-28 and 33-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,24-28,33,34* is/are rejected.

7)☒ Claim(s) *35 and 36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office Action is in response to applicant's communication filed May 31, 2005 in response to PTO Office Action dated December 8, 2004The applicant's remarks and amendment to the specification and/or claims were considered with the results that follow.

Claims 1-9, 24-28, and 33-36 have been presented for examination in this application. In response to the last Office Action, claims 5, 6, 9, 28, and 33 have been amended. Claims 35 and 36 have been added.

Claim Objections

Claims 35 and 36 are objected to under 37 CFR 1.75 as being a substantial duplicate of claims 5 and 6, respectively. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-4, 25, 26, 33, and 34 are rejected under 35 U.S.C. 102(e) as being anticipated by Bass et al. (US# 6,460,120)

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 1, Bass et al. teaches, as seen in Figure 13, **multiple (N) different memories** such as DRAM memories. Each of these memories is attached to an associated one of the multiple **(M) different buses**, which inherently facilitate data movement according to a certain bandwidth. A plurality of arbiters **(different memory controllers)** are coupled to the multiple different memories, and these different memory controllers comprise the TSM **Arbiter**. The plurality of arbiters of the TSM Arbiter control the accessing of the memories, as well as the modes for accessing the memories. The memories can be **set into two modes of operation** (col. 24, lines 36-63). Bass et al. further teaches that the memories are logically divided into sub-memories, and that these sub-memories can be logically **accessed simultaneously**. The arbiter of Bass et al. allows for such accesses in the form of writes or **read accesses** (col. 25, lines 10-18). The **access vector** as claimed refers to the logical address translation for data from the memory that must inherently occur due to the logical division of the memories and the associated logical simultaneous access. Although the Bass et al. reference does not specifically recite bandwidth in terms of the busses and memories, Bass et al. teaches that data can be read from the memories, which would inherently mean that the data travels at some speed relative to the bandwidth of the busses. Since Bass et al. also teaches that multiple memories may be read from simultaneously, the multiple pieces of data will be read over the multiple buses at the same time. Thus, **total bandwidth of all of the separate busses** related to the simultaneous read access is inherently **greater than the bandwidth of an individual bus** in the Bass et al. invention.

Regarding claim 2, Bass et al. teaches that the first mode may be a **read mode**, which is a sub-section of the TDM-mode in the form of read-only (col. 24, lines 59-63).

Regarding claim 3, Bass et al. teaches that the memory options may include multi-bank **DDR DRAM** (col. 9, lines 46-48).

Regarding claim 4, Bass et al. teaches partitioning the memory into at least **four banks with a buffer spread across the four banks** (col. 9, lines 55-60).

Regarding claim 25, Bass et al. teaches, as seen in Figure 13, **multiple (N) different memories** such as DRAM memories. Each of these memories is attached to an associated one of the multiple **(M) different buses**, which inherently facilitate data movement according to a certain bandwidth. A plurality of arbiters **(different memory controllers)** are coupled to the multiple different memories, and these different memory controllers comprise the TSM **Arbiter**. The arbiters of the TSM Arbiter control the accessing of the memories, as well as the modes for accessing the memories. The memories can be **set into two modes of operation** (col. 24, lines 36-63). Bass et al. further teaches that the memories are logically divided into sub-memories, and that these sub-memories can be logically **accessed simultaneously**. The arbiter of Bass et al. allows for such accesses in the form of writes or **read accesses** (col. 25, lines 10-18).

Regarding claim 26, although the Bass et al. reference does not specifically recite bandwidth in terms of the busses and memories, Bass et al. teaches that data can be read from the memories, which would inherently mean that the data travels at

some speed relative to the bandwidth of the busses. Since Bass et al. also teaches that multiple memories may be read from simultaneously, the multiple pieces of data will be read over the multiple buses at the same time. Thus, **total bandwidth of all of the activated separate busses** related to the simultaneous read access is inherently **greater than the bandwidth of an individual bus** in the Bass et al. invention.

Regarding claim 33, Bass et al. teaches, as seen in Figure 13, **multiple (N) different memories** such as DRAM memories. The DRAMs are divided (**partitioned**) into multiple **sectors** (submemories). Each of these memories is attached to an associated one of the multiple **(M) different buses**, which inherently facilitate data movement according to a certain bandwidth. Bass et al. **teaches partitioning the memory** into at least **four banks with a buffer spread across the four banks** (col. 9, lines 55-60). A plurality of arbiters **(memory controllers) are coupled to the multiple different memories**, and these different memory controllers comprise the TSM **Arbiter**. The plurality of arbiters of the TSM Arbiter control the accessing of the memories, as well as the modes for accessing the memories. The memories can be **set into two modes of operation** (col. 24, lines 36-63;). Bass et al. further teaches that the memories are logically divided into sub-memories, and that these sub-memories can be logically **accessed simultaneously**. The arbiter of Bass et al. allows for such **write control signals** for **accesses in the form of writes** or read accesses (col. 25, lines 5-31).

Regarding claim 34, The TSM Arbiter responds to a **read signal** for read accesses from any (**another**) **of the at least two of said N different memory** elements (col. 5, lines 25-31).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 24 is rejected under 35 U.S.C. 103(a) as being obvious over Bartoldus et al. (US# 6,560,227) in view of Bass et al. (US# 6,460,120).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the

application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Bartoldus et al., teaches a chip (controller) for **partitioning a frame** into **at least two parts (segments)**, where the segments are stored in N sets of 74 byte ping pong buffers (**plurality of memory elements)** (col. 2, lines 12-20). The segments are (**adjoining**) parts of the same frame, where the frame is sent over various LAN switches (**communication device**) and routing devices (col. 2, lines 1-11).

The difference between the claimed subject matter and that of Bartoldus et al., disclosed supra, is that claim 24 recites that an arbiter, in response to a request, causes data (parts) to be read simultaneously from the memory elements over separate busses.

Regarding claim 24, Bass et al. teaches, as seen in Figure 13, **multiple (N) different memories** such as DRAM memories. Each of these memories is attached to an associated one of the multiple **(M) different buses**, which inherently facilitate data movement according to a certain bandwidth. A plurality of arbiters **(different memory controllers)** are coupled to the multiple different memories, and these different memory controllers comprise the TSM **Arbiter**. The arbiters of the TSM Arbiter control the

accessing of the memories, as well as the modes for accessing the memories. The memories can be **set into two modes of operation** (col. 24, lines 36-63). Bass et al. further teaches that the memories are logically divided into sub-memories, and that these sub-memories can be logically **accessed simultaneously**. The arbiter of Bass et al. allows for such accesses in the form of writes or **read accesses** (col. 25, lines 10-18).

Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Bartoldus et al. and Bass et al. before him at the time the invention was made to modify the network system of Bartoldus et al. to include the simultaneous access memories of Bass et al., because then the requested data could be retrieved from the memories in a quicker fashion and use less processing cycles.

Claim 27 is rejected under 35 U.S.C. 103(a) as being obvious over Bartoldus et al. (US# 6,560,227) in view of Bass et al. (US# 6,460,120) and Applicant's Admitted Prior Art (AAPA).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed

in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Bartoldus et al., teaches a chip (controller) for **partitioning a frame** into **at least two parts (segments)**, where the segments are stored in N sets of 74 byte ping pong buffers (**plurality of memory elements)** (col. 2, lines 12-20). The segments are (**adjoining**) parts of the same frame, where the frame is sent over various LAN switches (**communication device**) and routing devices (col. 2, lines 1-11).

The difference between the claimed subject matter and that of Bartoldus et al., disclosed supra, is that claim 27 recites simultaneously reading data from multiple memories where the total bandwidth output from the memories matches the bandwidth of a FAT pipe port on a communication device.

Regarding claim 27, Bass et al. teaches, as seen in Figure 13, **multiple (N) different memories** such as DRAM memories. Each of these memories is attached to an associated one of the multiple **(M) different buses**, which inherently facilitate data

movement according to a certain bandwidth. A plurality of arbiters **(different memory controllers)** are coupled to the multiple different memories, and these different memory controllers comprise the TSM **Arbiter**. The arbiters of the TSM Arbiter control the accessing of the memories, as well as the modes for accessing the memories. The memories can be **set into two modes of operation** (col. 24, lines 36-63). Bass et al. further teaches that the memories are logically divided into sub-memories, and that these sub-memories can be logically **accessed simultaneously**. The arbiter of Bass et al. allows for such accesses in the form of writes or **read accesses** (col. 25, lines 10-18), where the read accesses are part of a read **window**. Although the Bass et al. reference does not specifically recite bandwidth in terms of the busses and memories, Bass et al. teaches that data can be read from the memories, which would inherently mean that the data travels at some speed relative to the bandwidth of the busses.

AAPA teaches that **FAT pipes** are high bandwidth channels for transmitting large amounts of data, and can be included in high-speed storage subsystems (page 2, lines 6-10).

Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Bartoldus et al., Bass et al., and AAPA before him at the time the invention was made to modify the network system of Bartoldus et al. to include the simultaneous access memories of Bass et al. and FAT pipe bandwidth of AAPA, because then the requested data could be retrieved from the memories in a quicker fashion and use less processing cycles according to the simultaneous access and FAT pipe features.

Allowable Subject Matter

Claims 5-9 and 28 are allowed over the prior art of record.

Response to Arguments

Applicant's arguments filed May 31, 2005 have been fully considered but they are not persuasive.

On page 14, paragraph 4 of the May 31, 2005 response the Applicant indicated that "The Bass et al. reference does not teach, among other things, a single arbiter performing the function set forth in the claims". Although the Applicant has not indicated as to which claims this argument applies, the Examiner believes the argument is directed towards at least the independent claims. As noted above by the Examiner, the single TSM arbiter comprises multiple memory arbiters that perform the operations as claimed in the independent claims, further discussed above and seen in Figure 13 of the Bass et al. reference (emphasis added).

On page 14, paragraph 4 of the May 31, 2005 response the Applicant indicated that "With respect (to) Claim 4 the reference does not teach at least one buffer spreading across at least four banks as recited in the claims". As noted above in the section of Bass et al. used for the rejection for claim 4, each buffer can be comprised of a pair of 2Mx16bitx4 bank DDR DRAM. (emphasis added). Therefore, the buffer could be comprised two 4-bank DDR DRAM memories. Also, the claim does not prohibit the claim interpretation that the buffer comprises the 4 banks of DDR DRAM.

On page 14, paragraph 4 of the May 31, 2005 response the Applicant indicated that "Regarding claim 33, the claim was recited at least one buffer spread across said multiple sectors". The Examiner has recited above in the claim rejection that the multiple sectors are interpreted as submemories, and as recited in the previous paragraph each DDR DRAM comprises 4 banks (submemories or 'multiple sectors'). The multiple sector partitions as claimed in claim 33 can be interpreted akin to the memory partition banks of claim 1, and as disclosed in the previous paragraph a buffer comprises the four banks (the buffer is 'spread across' the 'multiple sectors', where each memory inherently requires memory sectors to store data).

On page 14, paragraph 7 and paragraph 1 of page 15 of the May 31, 2005 response the Applicant indicated that a prima facie case of obviousness as required under 35 U.S.C. 103 was not completed by the Examiner, in that the "...Bass et al. reference does not teach a single arbiter performing the function set forth in the last element of Claim 24" and "... the last element of the claim which calls for a single arbiter performing the function set forth in the claim would not be present I the examiner combination". The Bartoldus et al. reference was not included in the rejection to teach the single arbiter. As previously noted by the Examiner, the Bass et al. TSM arbiter comprises multiple arbiters for performing the claimed operations, and as noted by Bass et al. the four banks of the DDRAM may be logically accessed simultaneously (col. 25, lines 16-18, found above in relation to claim 24).

Applicant indicated in paragraph 2 of page 15 of the response that "...new claims 35 and 36 are based on claim 3 written in disjunctive format. Therefore, claim 3 yields

the two new claims, resulting from claim 6 being dependent on it." Although the Examiner agrees that new claims 35 and 36 are based on claim 3, new claims 35 and 36 are also duplicates of claims 5 and 6, respectively, and are thus objected to and not indicated as being allowable over the prior art of record.

Applicant has indicated in paragraph 3 of page 15 that the "...argument on sufficiency of the declaration is in error" and "...if the examiner persists with the rejection applicants in subsequence document, such as an appeal, will address the issue that Bass et al. should not be considered as prior art in view of the affidavit which applicants believed in sufficient". The Examiner still believes that the applicant has not yet provided a satisfactory showing that would lead to a reasonable conclusion that the applicant is the inventor as required by MPEP 716.10, as previously recited by the Examiner in the December 8, 2004 Office Action, and encourages the Applicant to address the issue in an upcoming communication.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

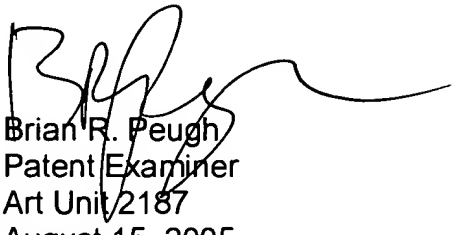
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is (571) 272-4199. The examiner can normally be reached on Monday-Thursday from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Brian R. Peugh
Patent Examiner
Art Unit 2187
August 15, 2005